


Getting You To Market Faster

VLSI Corporate Presentation Overview

Who Are We

Today's ASIC Challenge

Leveraging Our Capabilities

Conclusion

VLSI Technology

Who Are We

VLSI Milestones

1979
Founded

1982
First prototype Macintosh for Apple

1982
First automated design tools

1983
First Fabrication facility in San Jose

1988
San Antonio fab opens

1987
1st Digital Video Interactive chips

1990
Founder of ARM LTD.

1992
1st Dual-mode wireless phone chips

1994
Licensed DSP core from DSP Group, Inc.

1997
Special chips for IBM's Deep Blue

1998
Single chip wireless CDMA

1997
Single-chip wireless GSM

VLSI Financial Overview

- **U.S. $712 Million Revenue in 1997**
- **U.S. $95.5 Million Operating Income in 1997**
- **14.5% Of Revenue Invested In R&D in 1997**
- **$240 Million Capital Investment in 1997**

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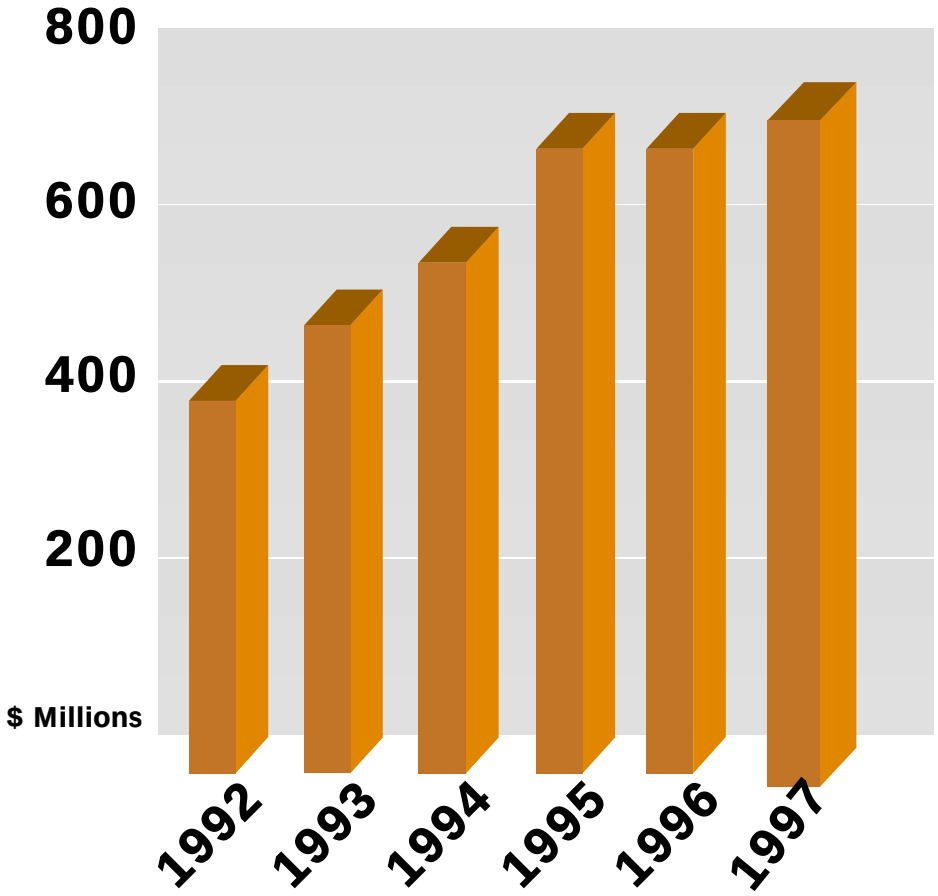
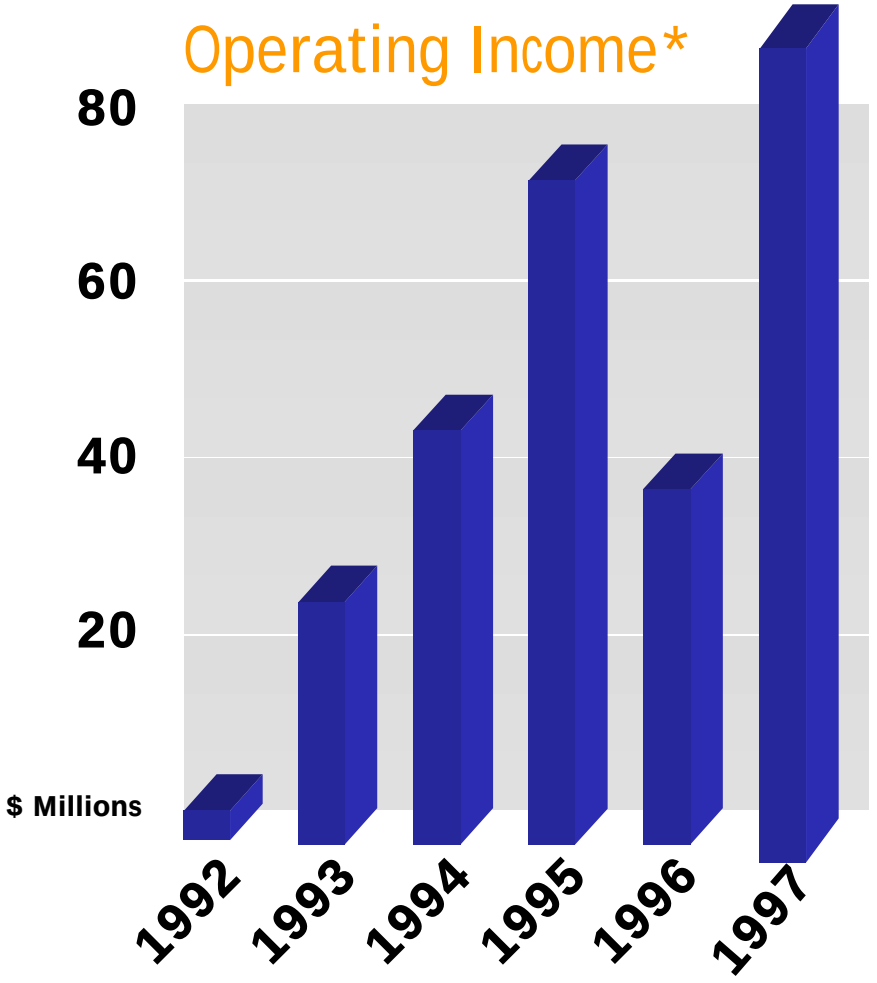
Revenue and Profits

Revenue



Operating Income*



* Excluding impact of Q492 and Q496 special charges

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Recent Results ($M)

($ Millions, Except EPS)	Q297	Q397	Q497	Q198	Q298
Revenue	171.0	181.2	193.0	141.3	137.8
Gross Margin % Revenue	71.5 41.8%	80.9 44.7%	87.1 45.1%	58.3 41.3%	52.8 38.3%
Operating Profit % Revenue	20.4 11.9 %	27.2 15.0 %	30.8 15.9 %	4.0 2.9 %	3.7 2.7%
Net Income from continuing operations	13.3	20.8	22.0	3.2	6.5
EPS from continuing operations	0.28	0.42	0.45	0.07	0.14
Gain (Loss) from discontinuing operations	(0.9)	7.7	-	-	-
Total EPS	0.26	0.57	0.45	0.07	0.14

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VLSI - Infrastructure

- Technology Centers and Sales Offices: 23
  - United States (15), Europe (4), Japan (2), Asia Pacific (2)
  - 175 Field based engineers for local customer support
- Product Development Locations Worldwide: 6
  - North America - San Jose, California; Tempe, Arizona; Vancouver, Canada
  - Europe - Sophia Antipolis, France; Rennes, France
- Manufacturing: 2
  - San Antonio
  - Pilot Line San Jose

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Our Market Segments

- **VLSI Has Focused Its Technical, Marketing and Sales Resources in Three Key Market Segments**
  - **Wireless Communications**
  - **Networking Communications**
  - **Consumer Digital Entertainment**
- **Resources also focused on emerging markets through our Internet & Secure and ASIC business units**




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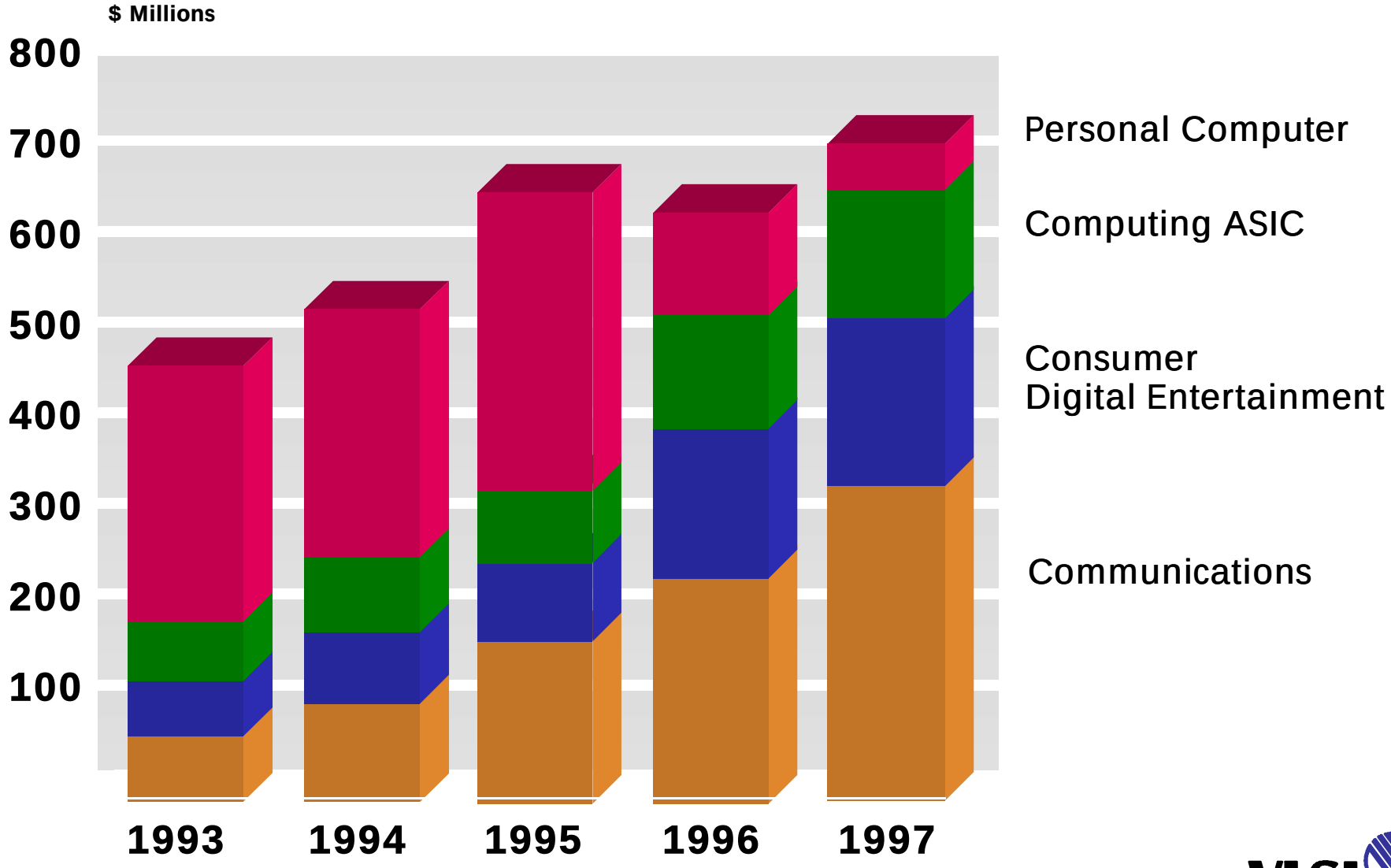
A Market Transformation
VLSI Revenue Trend



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Today's ASIC Challenge

Market Environment - Year 2000

- **Consumerization of Digital Products**
  - **Fast time-to-market**
  - **Short life cycle**
  - **Rapid design refresh**
  - **Need for silicon customization**

- **Design Challenges With Systems-on-a-chip / Multi-million Gate Designs**
  - **Multiple processors need HW / SW co-development**
  - **IP integration requires design reuse and system level silicon development strategies**
  - **Integrated communications capability**
- **VLSI Focused on Fast Delivery of Highly Integrated, Customized Semiconductors**

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Market Environment - Year 2000

- **More Embedded Processors**
  - **In the year 2001, approximately 80% of system IC designs will have embedded CPU and 30% will have multiple CPU's - IBS IP report 1/98**

  - **25% of all ASIC designs will use an ARM by the year 1999 - Dataquest user survey 12/97**
  - **DSP statement to come**

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The Design Gap

- **System-on-a-Chip Designs vs. Moore's Law**
  - **Potential = 8 million transistors - 59% CAGR**
  - **Actual average design = 1 million transistors - 25% CAGR**

- **Why? - Customers Unwilling to Risk Larger System**
  - **Can't verify the system**
  - **Must meet product schedule**
- **Design Tools, Methodology - Limiting Factors**

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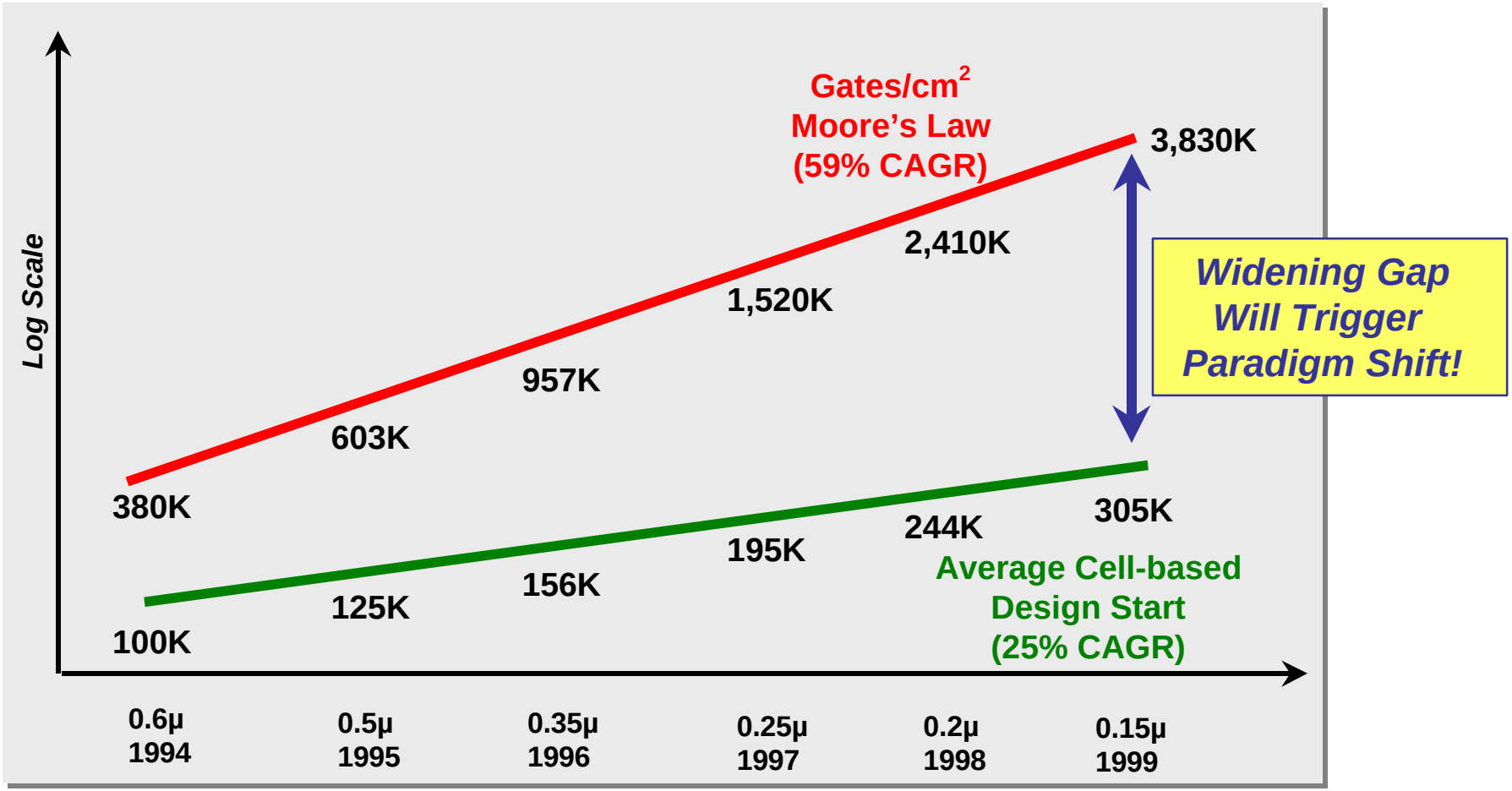
Design Productivity Gap



- **Growing Gap Between What's Designable and What's Manufacturable**

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Leveraging Our Capabilities

Leveraging VLSI's Capabilities

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Methodology

- **VLSI Advanced Methodologies Give You the Fastest Time-to-System Silicon With the Lowest Risk…**
  - **HDLi design tool for IP reuse**
  - **Velocity Rapid Silicon Prototyping development systems to enable early system / application development**
  - **Design Integrator for seamless integration of industry leading tools to yield first-time-right silicon**
  - **Best-in-Class Design tools used in design centers**
  - **High-flex manufacturing optimized for fast prototype turns and volume ramp**

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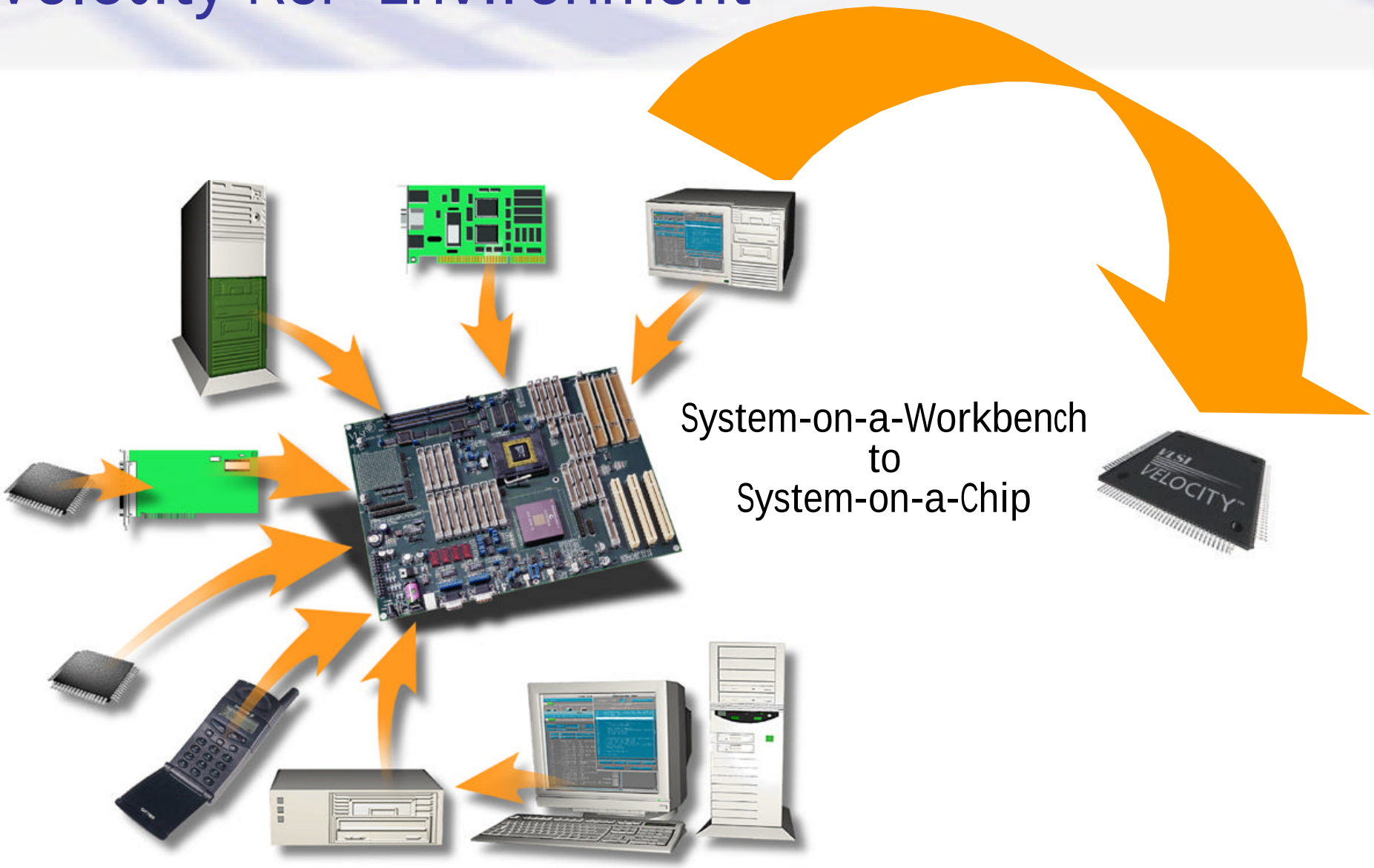
Velocity RSP Environment



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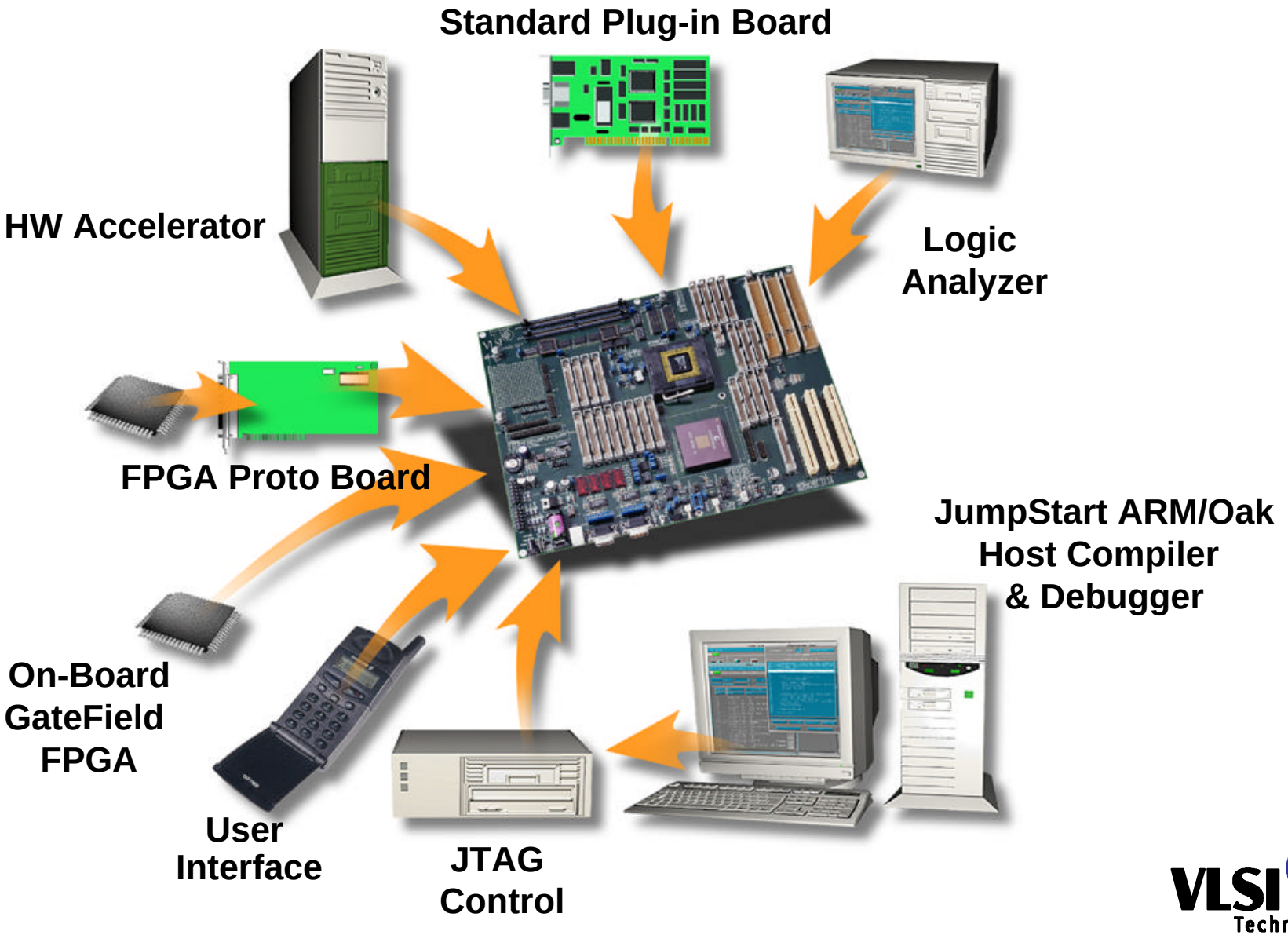
The RSP7 System-on-a-Workbench



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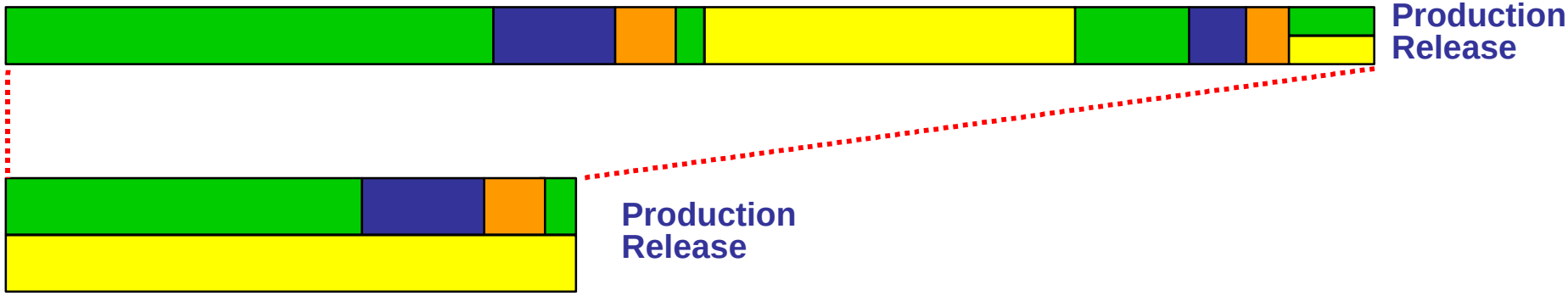
Design Cycle Benefits

Conventional Design Process



RSP Design Process

HW Development and Validation

Placement, Routing & Physical Verification

Silicon Fabrication

SW Development and Validation

- **Faster Chip Development**
- **Hardware-software Development in Parallel**
- **More Than 50% Total Design Cycle Reduction**

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A Real, Deliverable Solution

- **First Systems Now in Beta**
- **Available to Customers Q3**

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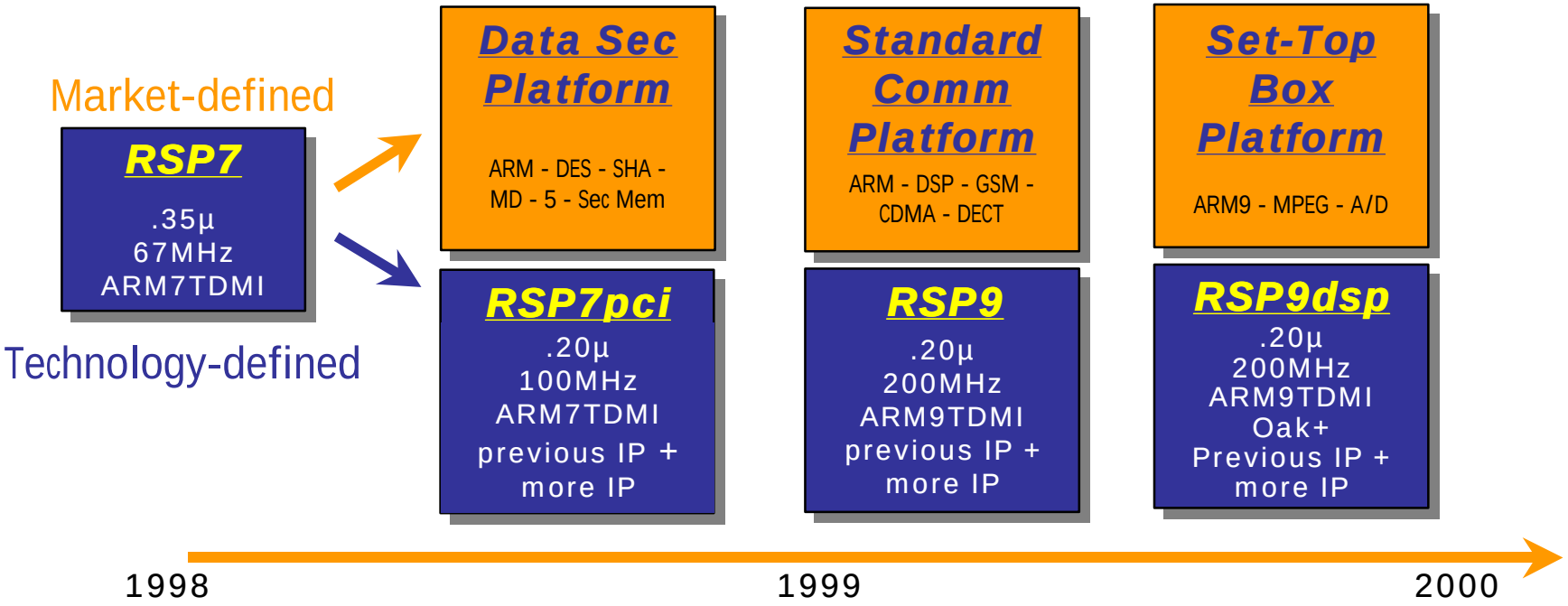
Robust Platform Roadmap



- **Technology defined platforms track ARM / Oak evolution, multicore architectures, additional buses**
- **Market defined platforms wireless communications, data security, set-top box, networking platforms**
- **Customer-defined platforms mixing in customer IP**

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Rapid Silicon Prototyping Key Benefits:

- **Enables Systems-on-a-chip**
- **Shortens Development Schedule and Reduces Cost**
- **Reduces Risk**
  - **Approach 100% “First Pass” Silicon Success**
- **Shortens Customers’ Time-To-Market**

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Core Technology

- **Process Technology**
- **Packaging**
- **Libraries**
- **Intellectual Property**

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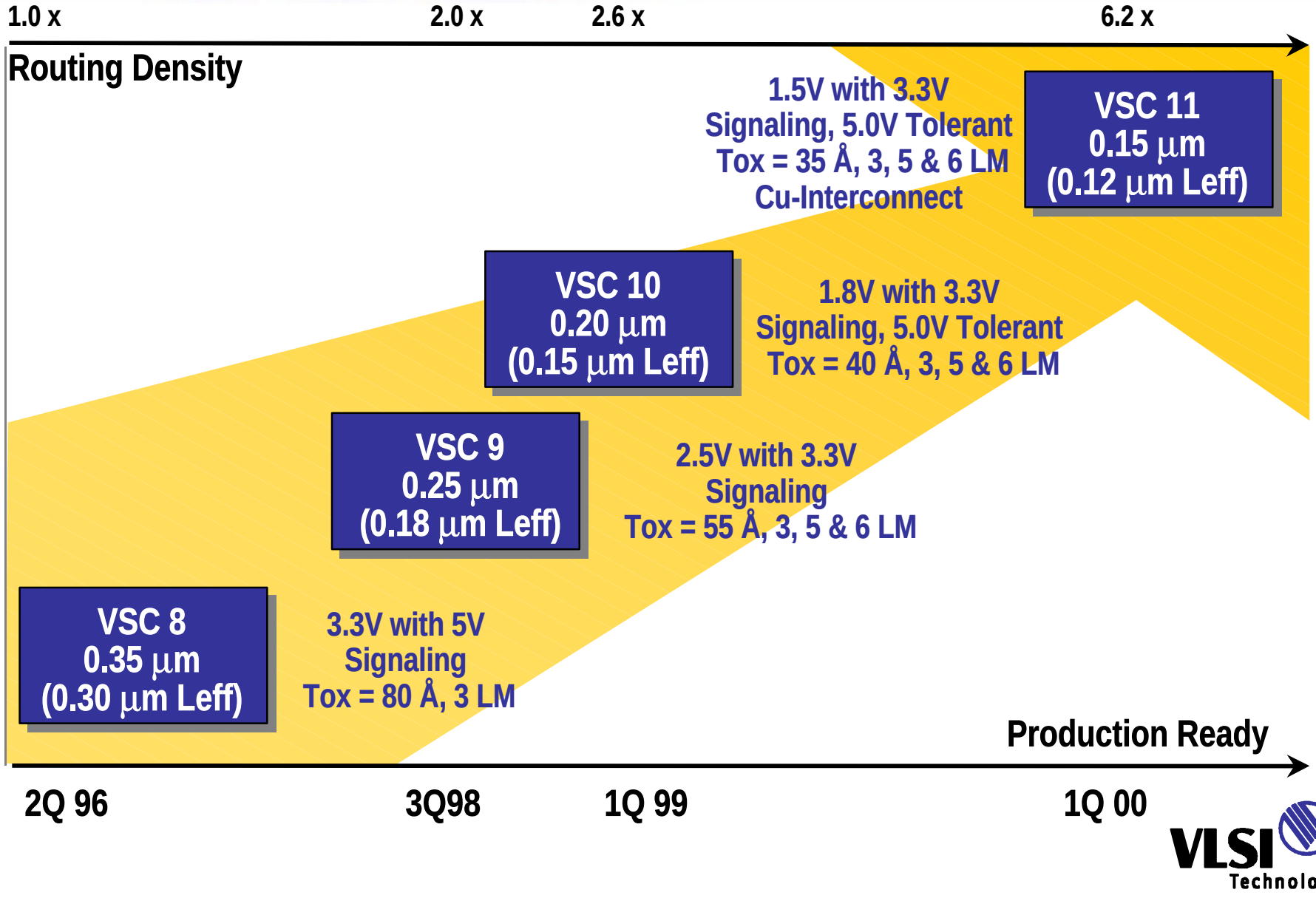
Technology Transitions



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Package Application Trends

Application	Technology
High Performance ASIC & Networking	FCBGA EPBGA HBGA
Wireless Communication	PBGA FPBGA FCCSP
Consumer Digital Entertainment/ Internet/Secure	PBGA FPBGA FCCSP QFP

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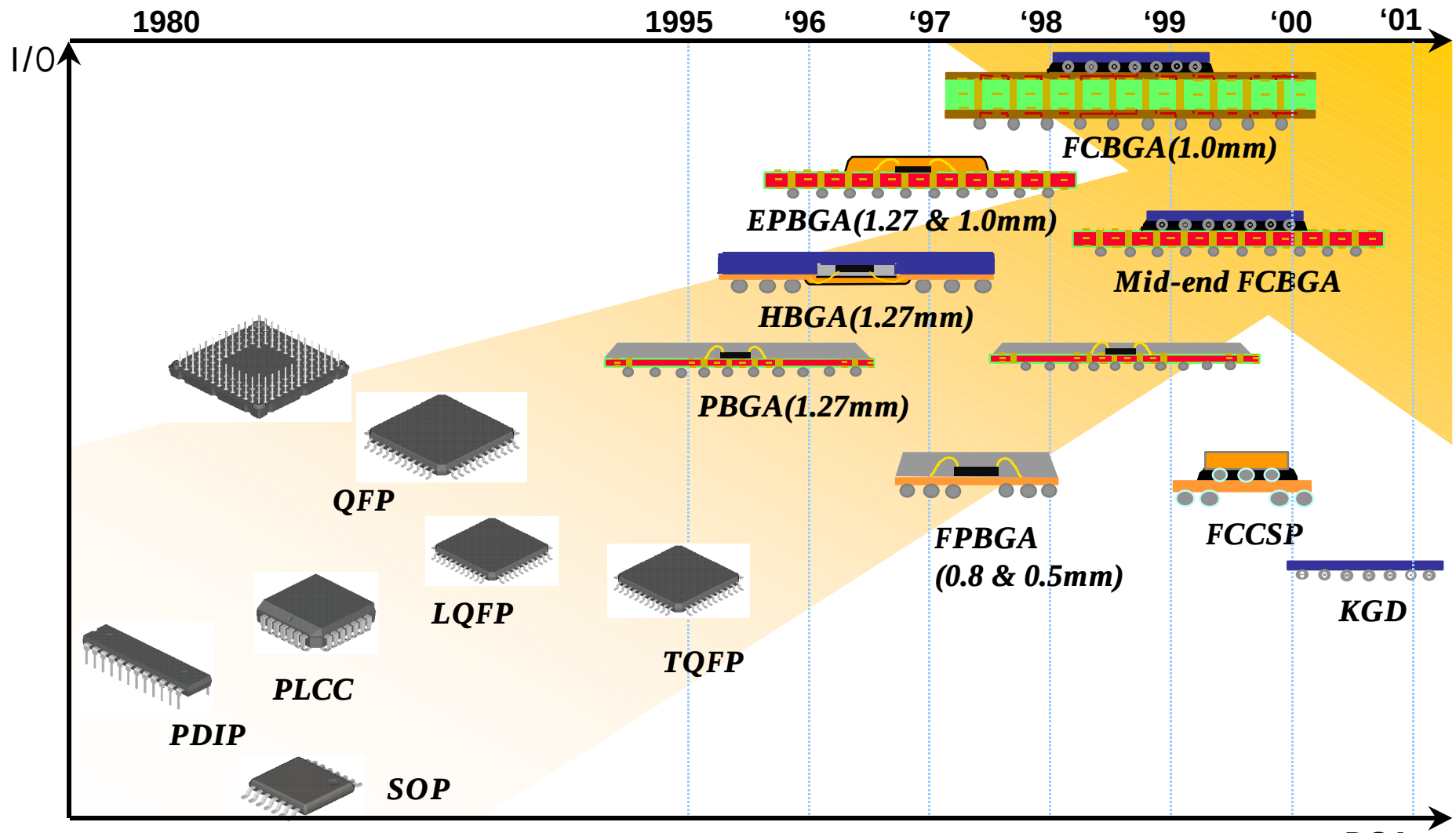
Package Technology Roadmap



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Cell Libraries

- **One of the Largest Core Libraries in the Industry**
  - **Synthesis optimized with full scan support**
  - **Comprehensive offering of 150 functions and 600 cells**
- **Multiple Drive Strength to Efficiently Satisfy Both High Performance and Low Power Requirements**
- **Hand Packed for Density While Offering Performance.**
- **Supports All Significant I/O Protocols: CMOS, TTL, PCI (33 &66 MHz), GTL, GTL+, SCSI, HSTL, SSTL, LVDS**
- **Flexible I/O Aspect Ratio Offering for Core Limited and Pad Limited Designs.**

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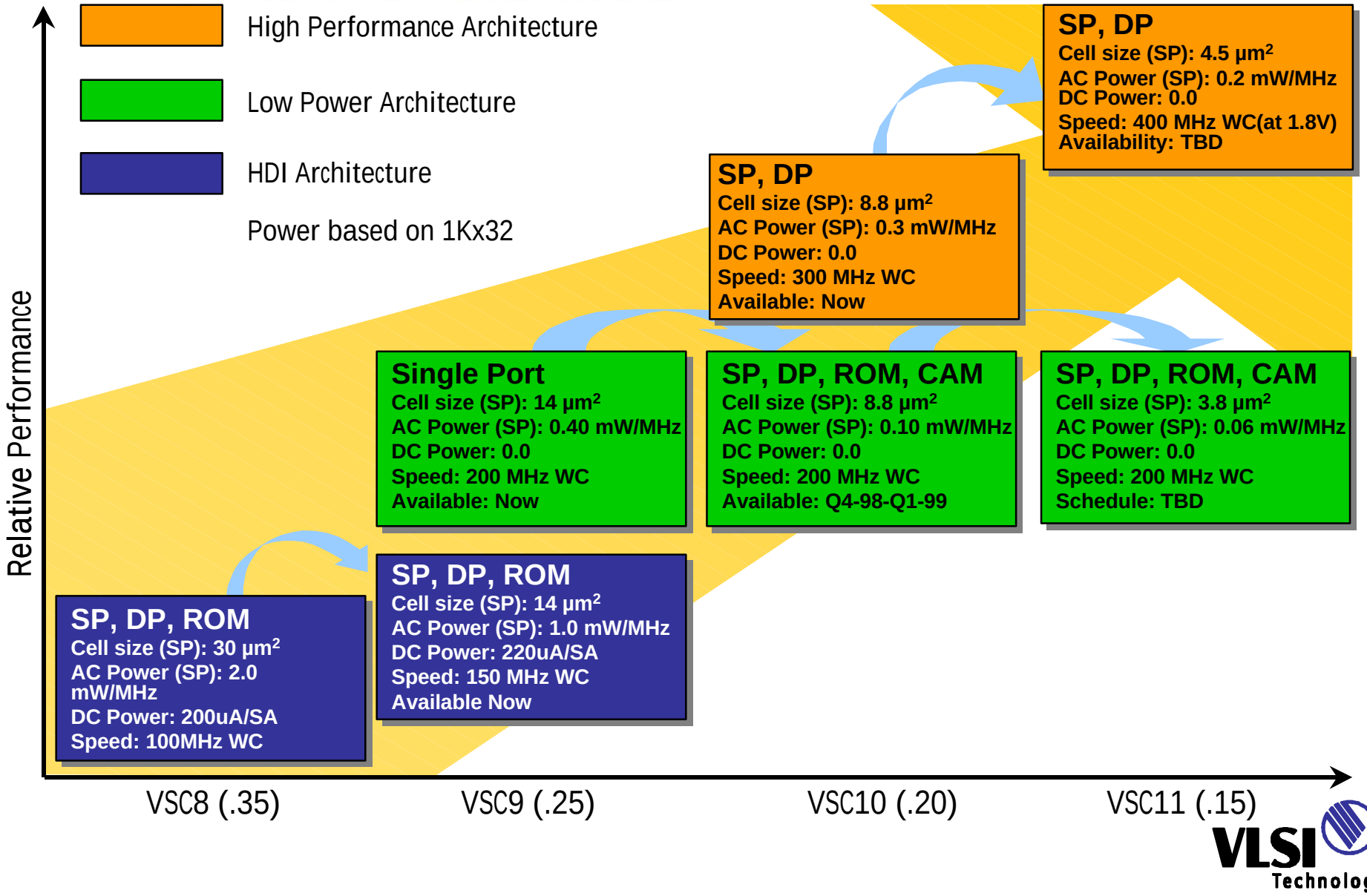
Memory Compiler Road Map



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Design Integrator

- VLSI's Open Design Environment -

- **Provides access to VLSI's advanced technology and enables System-Level Silicon design using a combination of VLSI proprietary tools and industry recognized EDA tools.**
- **Supports Verilog and VHDL at both HDL and gate level design.**
- **Contains standard cell, I/O, analog and memory compiler access for VLSI's leading edge technologies.**
- **Includes HDL Integrator, VLSI's IP delivery vehicle.**
- **Supports a sign-off environment for simulation tools.**
- **Provides a consistent timing view across all EDA tools.**
- **Uses standard formats for tool interoperability.**
- **Ensures compatibility of designs with VSLI's production test and manufacturing facilities.**

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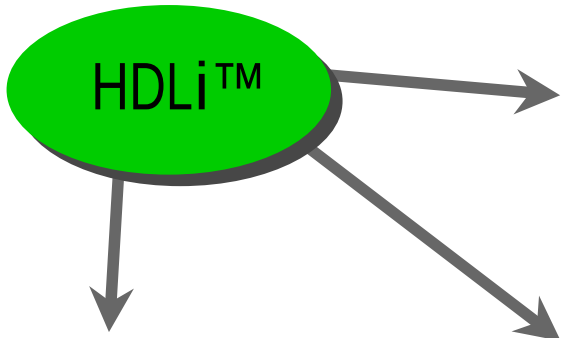
System Technology HDL Integrator™

A Tool for Design Reuse and Productivity



HDL Template Compiler

- **"Compilable FSBs"**
- **Generates mixed RTL and structural HDL implementation**
- **E.G., UART with programmable FIFO depth.**

Macro Compiler

- **Efficient compilation of macros, blocks or functions**
- **Generates both RTL and structural implementation**
- **E.G., Multipliers, LFSRS, Comparators, Regfiles, etc.**

FSB™ and SSB™ Distributor

- **Supports delivery of FSB™ and SSB™ databases**
- **E.G. ARM, Oak, FPA, ARM7TDMI, PLL, etc.**

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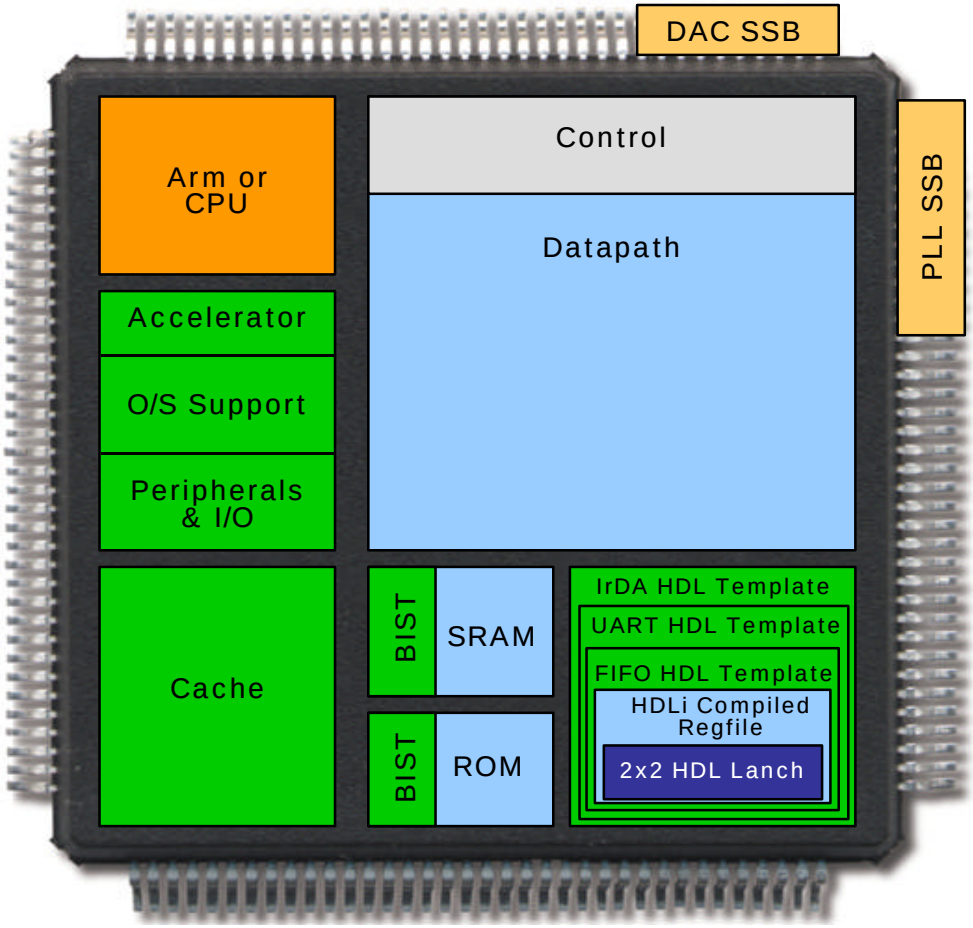
HDL Integrator (HDLi™) Example

A Complete Design Reuse Solution



- **Reuse = SSB™ Cells + FSB™ Cells + HDL Templates + compiled blocks**
- **HDL Templates will provide architectural efficiency by allowing users to remove unwanted features**
- **Efficiency is NOT sacrificed for productivity – you get both!**
- **We strive to achieve industry's best function- to technology mapping thru templates and compilers. We don't rely on Synthesizers alone to dictate silicon efficiency**
- **Complete Offering**
- **IP Libraries**
- **Flexible Solutions**

An example of how reuse builds on reuse to give silicon efficiency. Templates can call other templates which can call compilers ... which call special HDI macros that a general purpose synthesis tool would never use.

Many CAE vendors seem to view "design reuse" with only productivity in mind. We are focusing on productivity,efficiency, and flexibility

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HDLi™ Integrates into Design Flow

- **Supports Verilog and VHDL design flows**
  - **Outputs Verilog, VHDL, and NLS file formats**
- **Invoked by Design Integrator or stand-alone**
  - **Design Integrator Verilog**
  - **Design Integrator VHDL**
  - **Design Integrator Mentor**
- **Complements (does not replace) synthesis**

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HDLi™ Macro Compilers

- **More Efficient Implementations Than Synthesis**
  - **Lower net count (reduced interconnect effects)**
  - **Smaller**
  - **Faster**
- **Faster Time-to-Market**
  - **Shorter development and debugging time**
  - **Simplifies place and route**
- **Provides Algorithmic Expertise**
  - **Essential for datapath, DSP, and other computationally intensive apps.**
  - **Robust, highly tested macro algorithms**
  - **Simulation and synthesis tool independent**
  - **Supports industry standard HDL's Verilog and VHDL**

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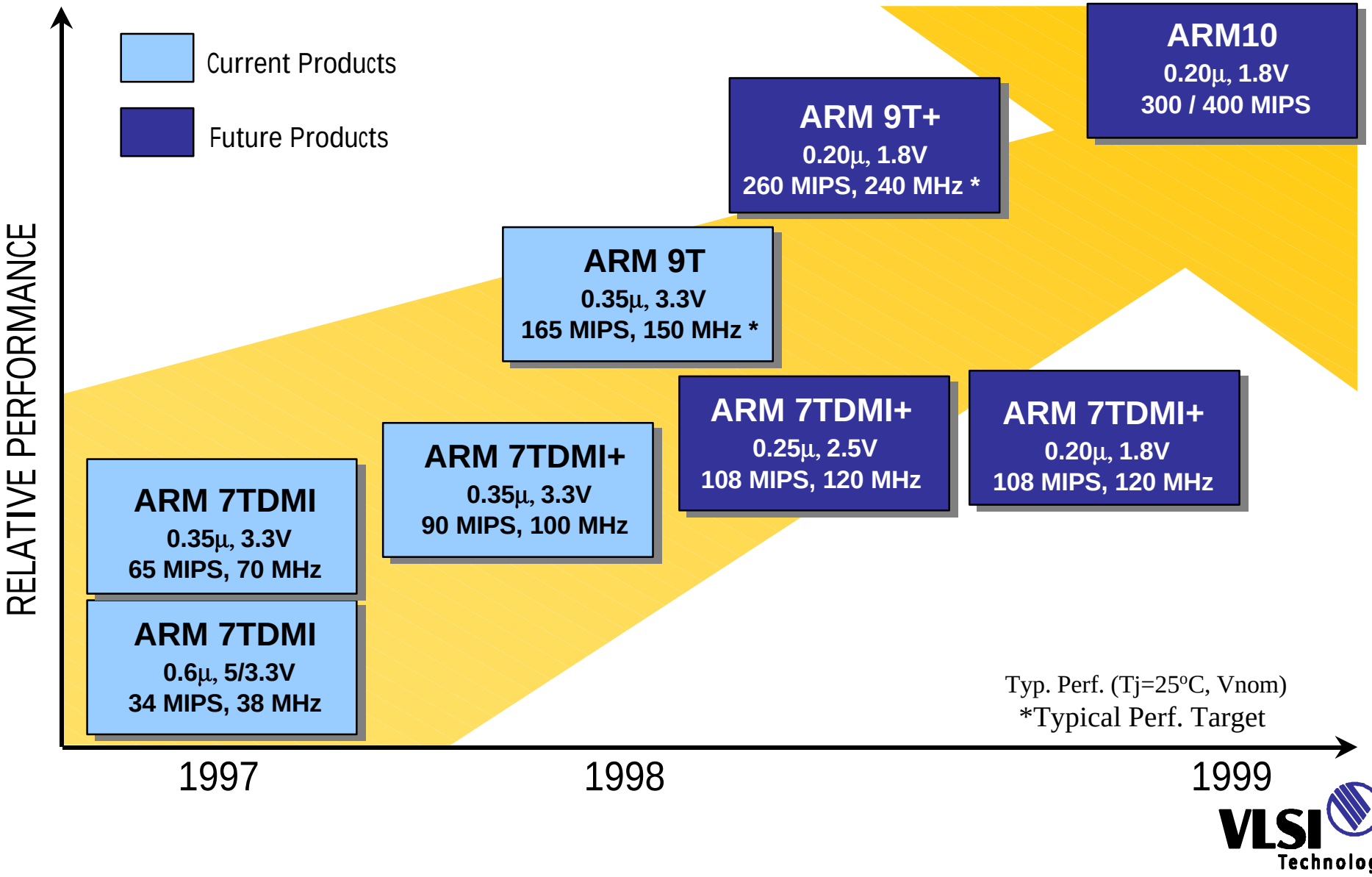
ARM Roadmap



Typ. Perf. (Tj=25°C, Vnom)
*Typical Perf. Target

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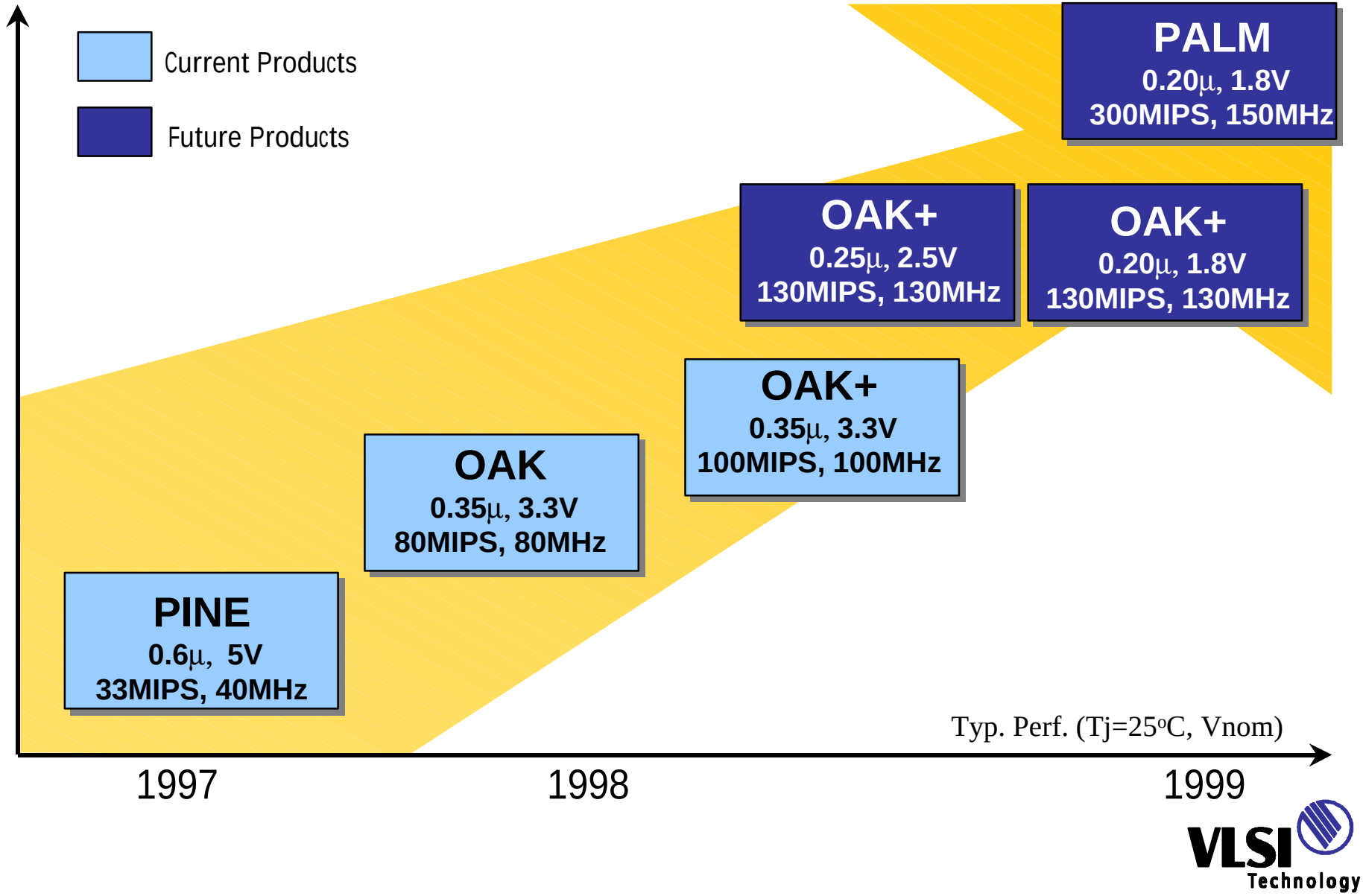
DSP Roadmap



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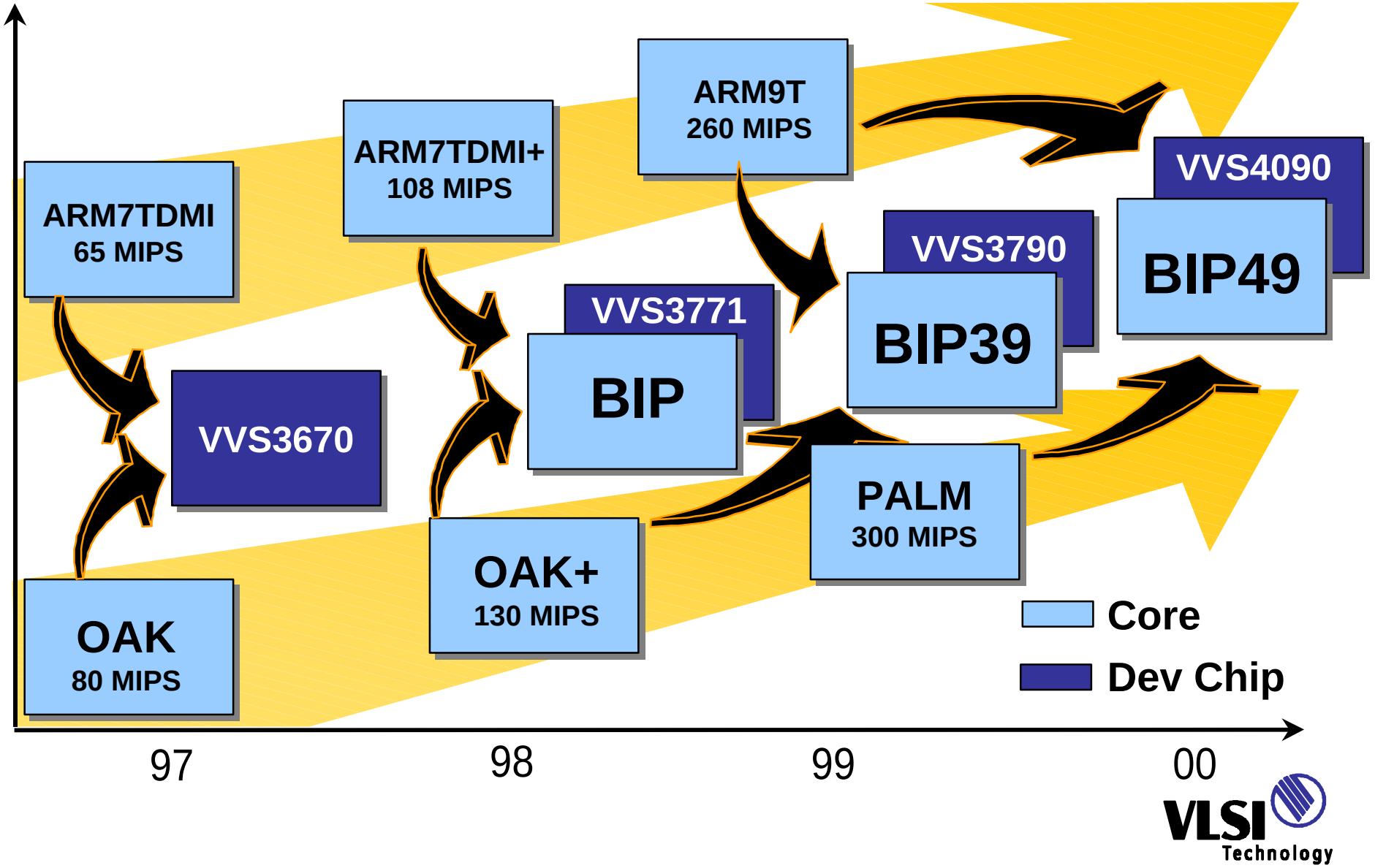
Multicore Roadmap



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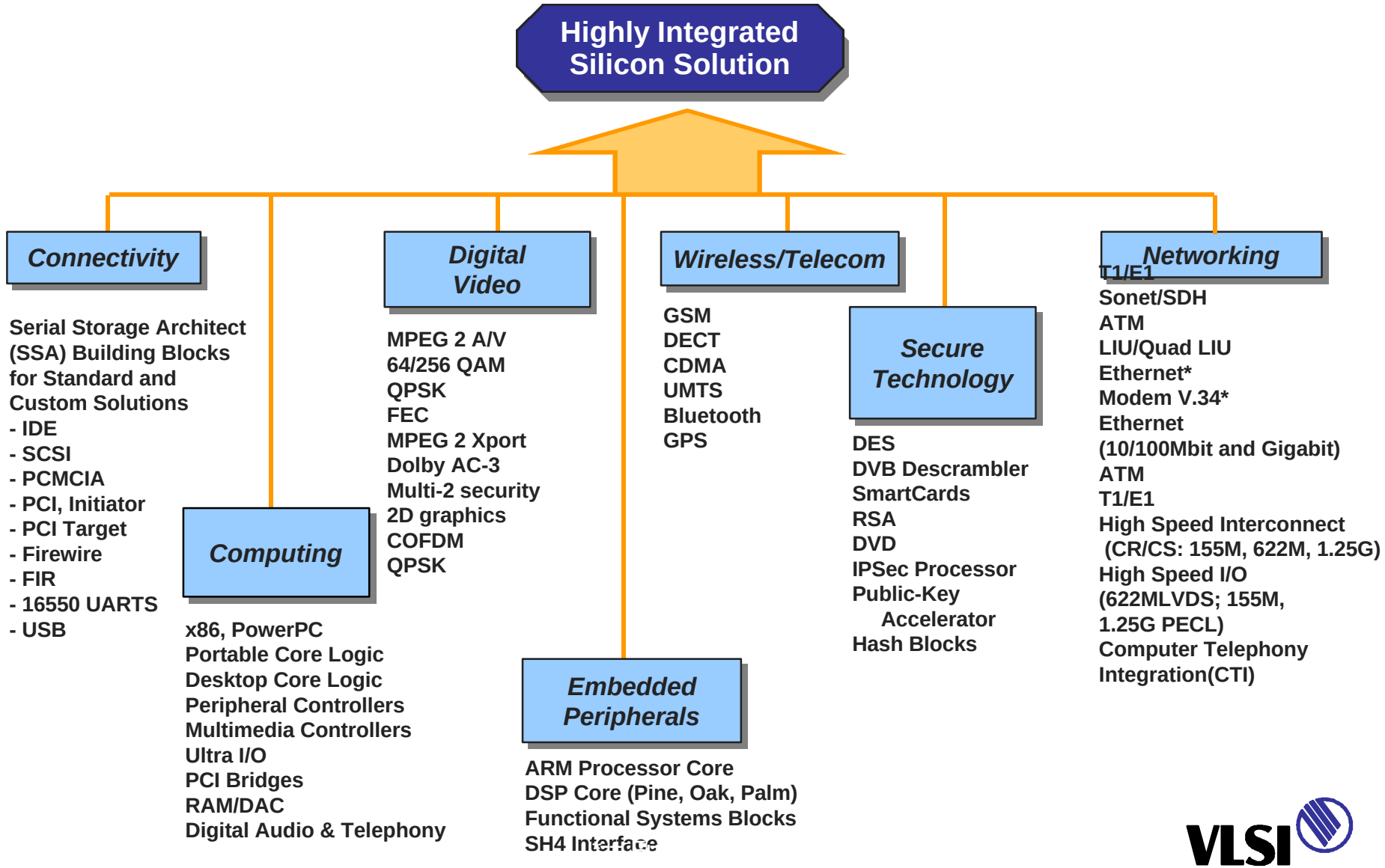
Technologies & FSBs™



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Mixed Signal Design

- **Capability**
  - **Standard digital CMOS process**
  - **Extensive library (e.g. Audio,video,RF)**
  - **Worldwide design capability**
- **Methodology**
  - **Cell characterization in silicon**
  - **Advanced test methodology**
  - **Application specific development**
- **Benefits**
  - **Low risk**
  - **Faster time-to-market**
  - **Reduced cost of ownership**
  - **Design re-use / technology migration**
  - **Compliant by design**
- **30% of all Digital Cellular Phones worldwide contain VLSI Analog Functions**

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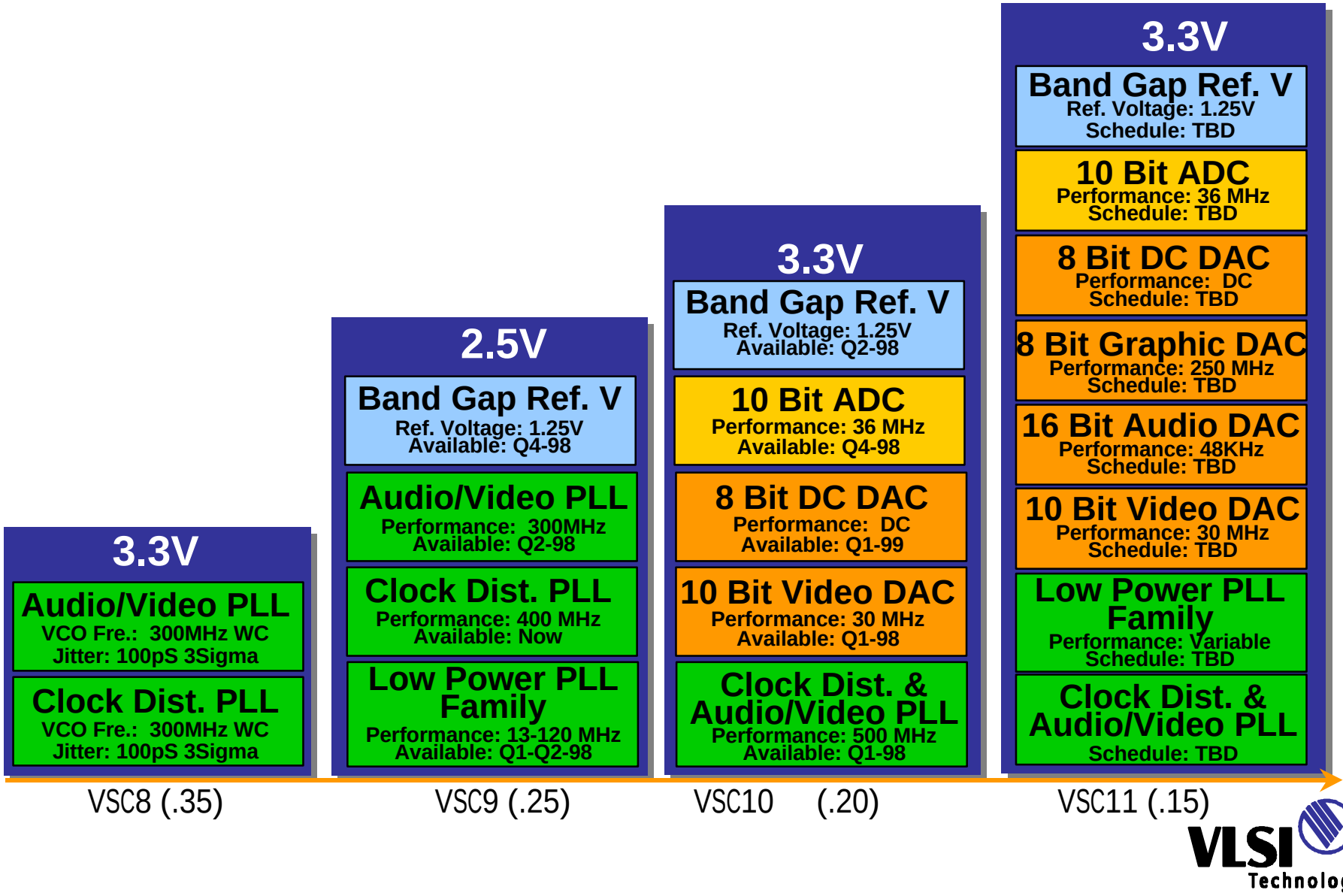
Analog Library Roadmap



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Manufacturing

- **VLSI owns and operates a world class “pure-play” ASIC fab in San Antonio, Texas that has been in operation for 10 years.**
- **Deep sub-micron wafer processing including 0.8µm, 0.6µm, 0.5µm, 0.35µm, 0.25µm and later in 1998 0.2µm.(1)**
- **From 2-layer metal up to 5-layer metal, 6 layers with flip-chip, allows the customer the highest possible degree of circuit integration and density.**
- **A leader in defect density and product quality.**
- **A leader in prototype and manufacturing cycle times.**
- **Foundry services available.**
- **Predictable output from an ISO 9002 certified Class 1 fab.**

(1) All features sizes stated as “drawn” dimensions. Electrical gate lengths are smaller.

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Technology Centers

15 International Locations

- U.S.
  - Atlanta, Chicago, Princeton, Baltimore, Colorado, San Diego, Boston, Dallas, San Jose, Raleigh, Irvine
- Europe
  - Munich, Germany; Milton Keynes,U.K.; Palaiseau, France
- Asia
  - Tokyo

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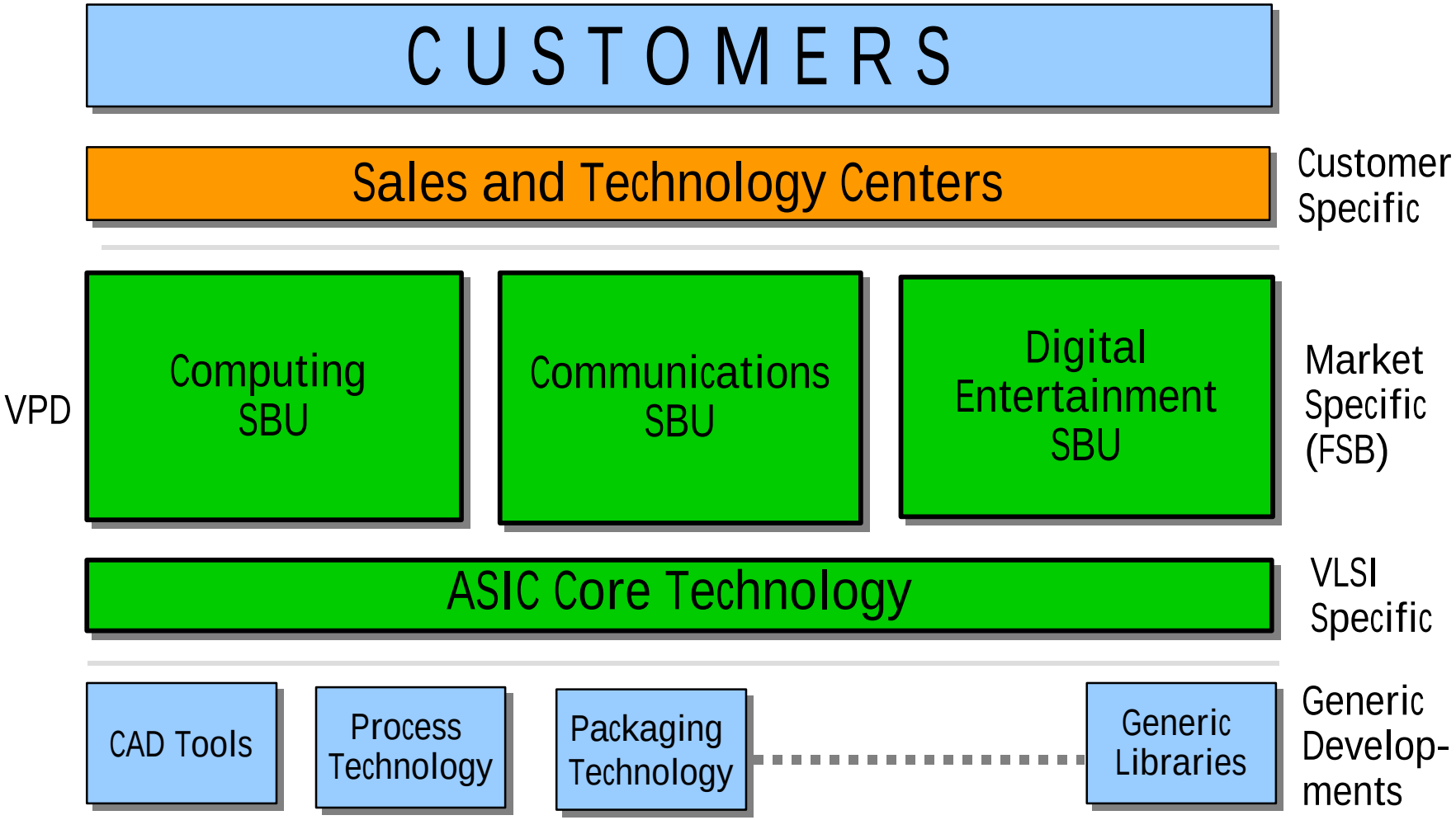
Technology Centers & Field Support Overview



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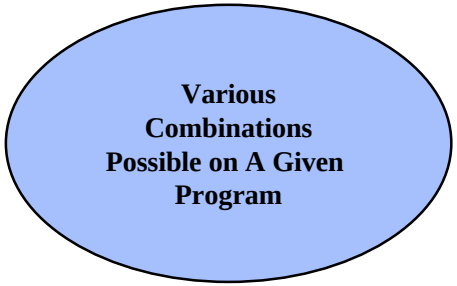
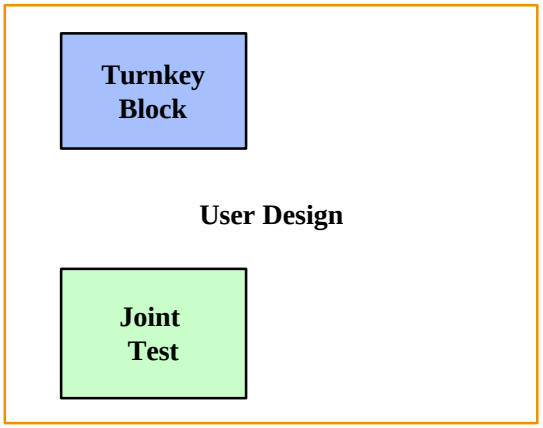
Design Support Scenarios

User Design

- **Design support on ASIC implementation**
  - Synthesis
  - Simulation
  - Layout
  - Test
- **Joint Design**
  - Design of custom blocks or cells
  - System and logic design support
  - Customer floorplanning
- **Turnkey Design**
  - Low & high complexity functions
  - Simulation & vector suites





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Technology Center Engineering Tasks

- **Design Consulting**
- **HDL coding and synthesis**
- **Turnkey Functional System Block Design**
- **Static and Dynamic timing analysis**
- **Performance, power, testability analysis**
- **Circuit and Logic design of specific macros / I/O structures**
- **Scan and BIST test insertion and pattern generation**
- **Design layout floorplanning and routing**
- **Physical verification and test/product engineering support**
- **EDA tool support**

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Worldwide Local Design Centers

- **Increase chance of first time right silicon and speed time to market by bringing the knowledge base from over 1000 standard cell designs close to the customer**
- **Provide chip integration consulting capability to the front end of the design process to help the customer:**
  - **Make design methodology decisions that ensure a predictable design process**
  - **Make partitioning and architectural tradeoffs to ensure performance targets are met**
- **Embedded processor systems expertise (over 250 designs) available in all Tech centers**
- **Applications expertise for VLSI target markets is located near trend setting customers**
- **Capacity to provide local customization of cores and blocks meet to individual design requirements**
- **Capabilities include all phases of an ASIC design**
- **Leverage leading edge, industry standard design tools which ensures predictable time to market success**

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Targeted Technology

- **Wireless**
- **Networking**
- **Consumer Entertainment**
- **ASIC / Computing**

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Wireless Market and Products: Overview

Velocity SCP, the Heart of Our Wireless Activities

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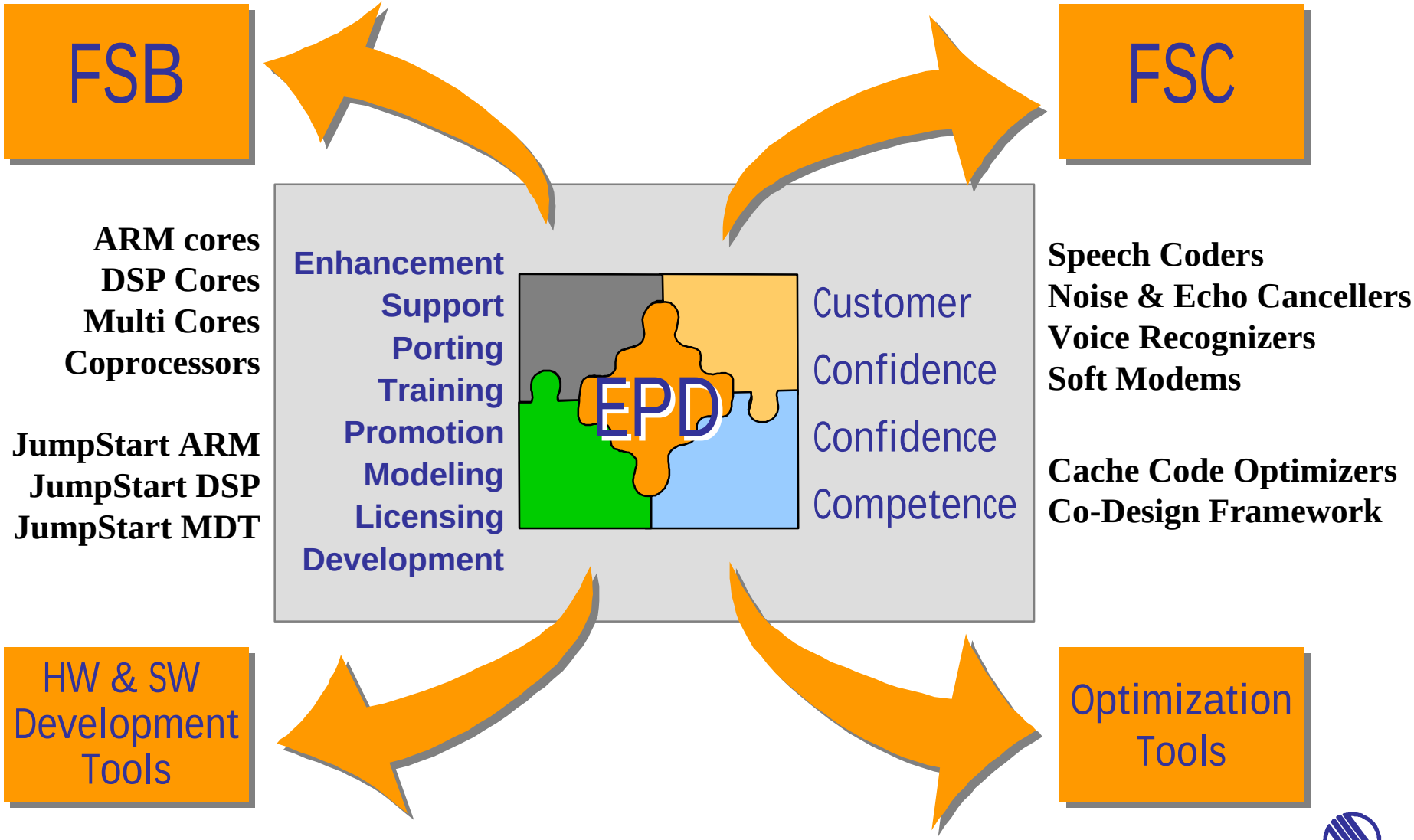
EPD MISSION



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Wireless Market and Products
Key Differentiators/Product Offering

- **Leading wireless chip supplier:**
  - **over 50M chips shipped**
  - **offer the dual-core Velocity, Standard Communication Platform for quick ASIC development**
  - **support GSM, CDMA and DECT standard product customization**
- **Cellular Expertise:**
  - **Provide the most highly integrated, cost-effective GSM solution: GSM 1C**
  - **Provide the first generation CDMA product: CDMA+ Processor 100**
  - **First company to propose solutions for both GSM and CDMA on the wireless market. Ready for Third Generation (UMTS).**
- **Leading-edge Cordless Solutions:**
  - **Vega, optimized DECT processor for handsets and residential base stations**
  - **Vmax, powerful DECT processor optimized for DECT Wireless Local Loop systems and PBXs**

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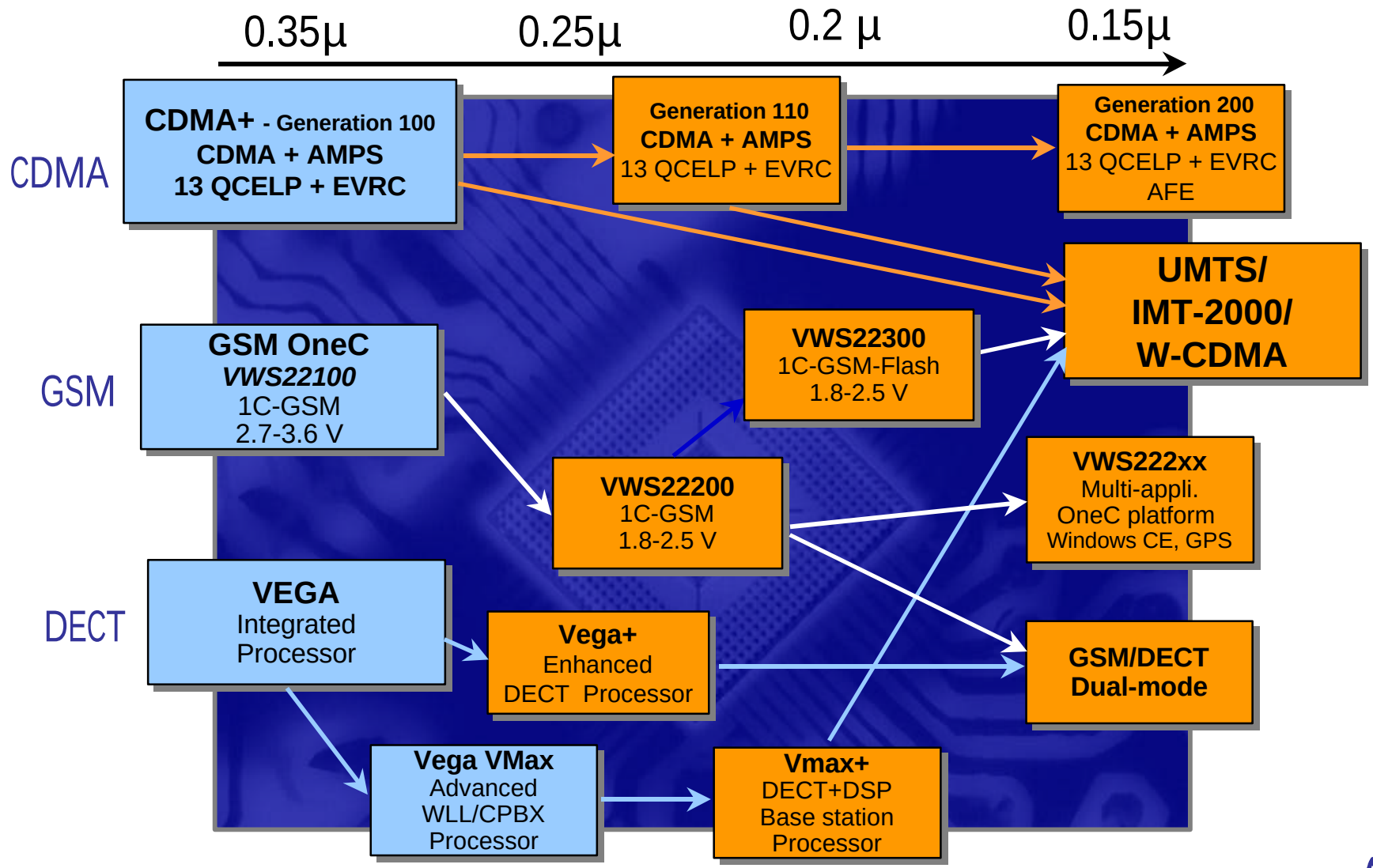
Wireless Market and Products Roadmap



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NPD Market and Products

- **Key Differentiators / Product Offerings**
  - Superior service to the major players in the form of design, CMOS technologies, misc. IP, and sales / marketing coverage**.**
- **VLSI's foundation of existing networking IP blocks**
  - HSI up to 1.25GbS, 10 / 100 MAC, 1Gb MAC, ARM RISC, Oak DSP, T1 Framer, HDLC controller, and other misc. IP.
- **Proactively procure / acquire IP blocks demanded by the major networking players**
  - E1 Framer, 10 / 100 phy, Gb Phy over fiber, Gb Phy over wire, HSI >2.5GbS, ADSL, etc.

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NPD Market and Products

NPD IP Blocks

IP Block	Synthesizable?	Comments
ARM 7	yes	Becoming prevalent in LAN space
10/100 PHY	no	first design implemented in .2um
10/100 MAC	yes	mainstream OEMs use proprietary MACs
622 HSI	portions	back plane
1.25 HSI	portions	back plane
Security	Yes	E-commerce driving IP from NICs to Routers
PCI	Yes	New standards developing for high speed PCI
CAM	yes	Still in development
Emb. flash	NA	Colloboration with Macronix in 0.2u
Emb DRAM	NA	In Development
Gb Cu Phy	NA	Looking for IP
QLIU	no	Gate level design. Limited reuse.
Palm DSP	yes	In final design stage.
Gb MAC	yes	Common MAC with Gb LAN.
2.5G HSI	Portions	Looking for IP
5.0G HSI	NA	Investigating Need
UTSI	NA	Investigating Need
UTOPIA	yes	Existing IP in previous generation process
Cell Del Blk	yes	Existing IP in previous generation process
ATM QUNI	yes	Existing IP in previous generation process
2048 HDLC	yes	In design
28 T1 framer	yes	In design, can be scaled back to handle fewer channels
De-jitter PLL	NA	Investigating Need
OCN Framer	NA	Investigating Need
HiFn	NA	Investigating Need
CTI	no	Very successful standard product. Use with SAFE?

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NPD Market and Products

Roadmap

A. 10/100 Phy →	Gb Phy (fiber) →	Gb Phy (wire)
B. 0.2um 1.0 GbS HSI →	2.5 GbS HSI →	5.0 GbS HSI
C. T1 (Safe) Framer HDLC Controller →	E1 Safe Low channel T1/E1 →	T/E1 Transceiver Dual Mode Framers
FY 99		FY 01

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Consumer Entertainment Market and Products

- **Overview**
  - **Focused on providing complete chipset solutions for implementing Digital Set-Top Box for Satellite, Cable & Terrestrial services worldwide.**

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Consumer Entertainment Market and Products

- **Key Differentiators / Product Offerings**
  - **System expertise**
  - **Complete solution from one vendor (hardware / software)**
  - **Custom ASIC Design Capability**
  - **Strong embedded CPU Roadmaps based on ARM**

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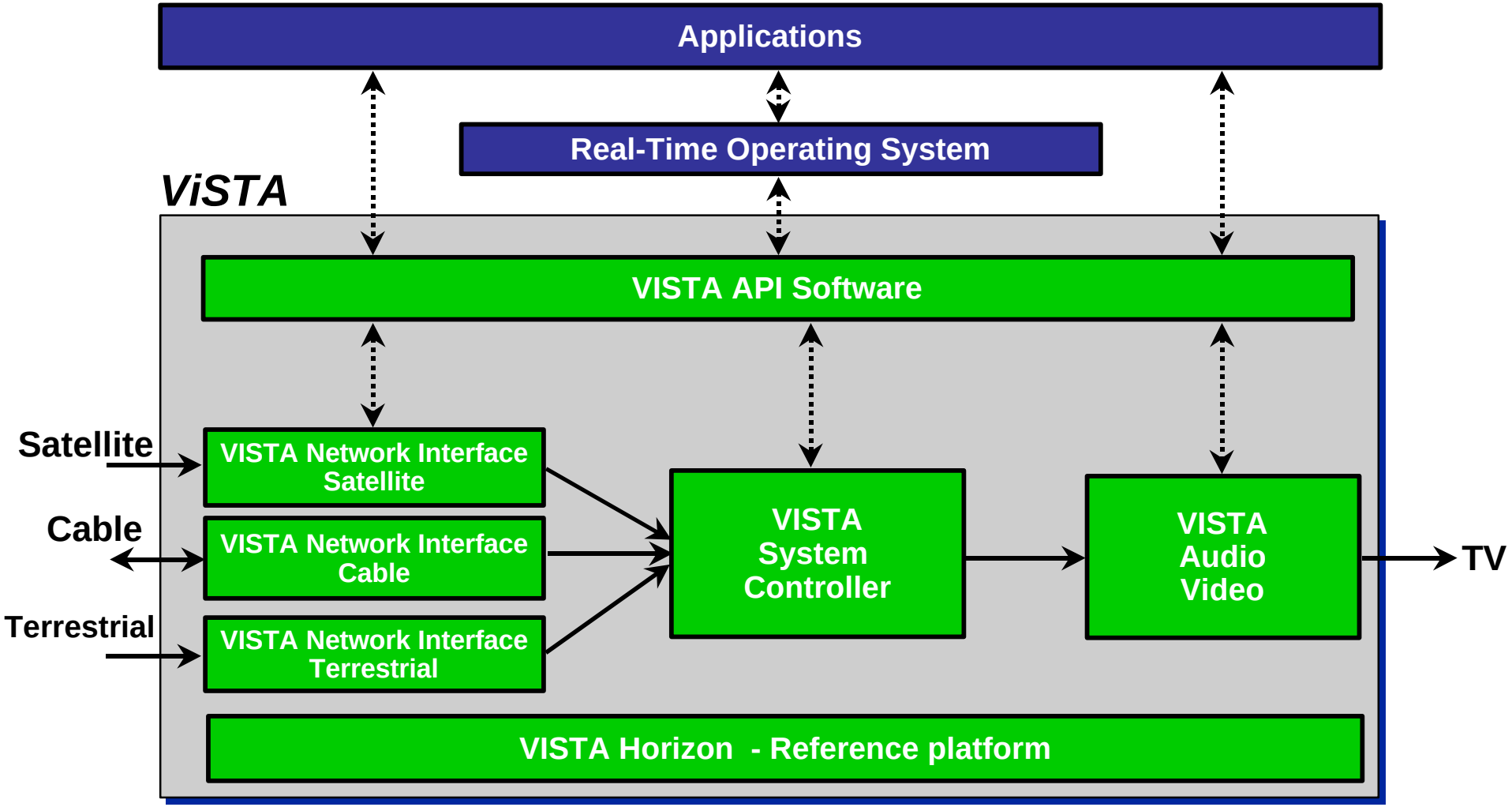
ViSTA Roadmap
ViSTA 1999 Architecture



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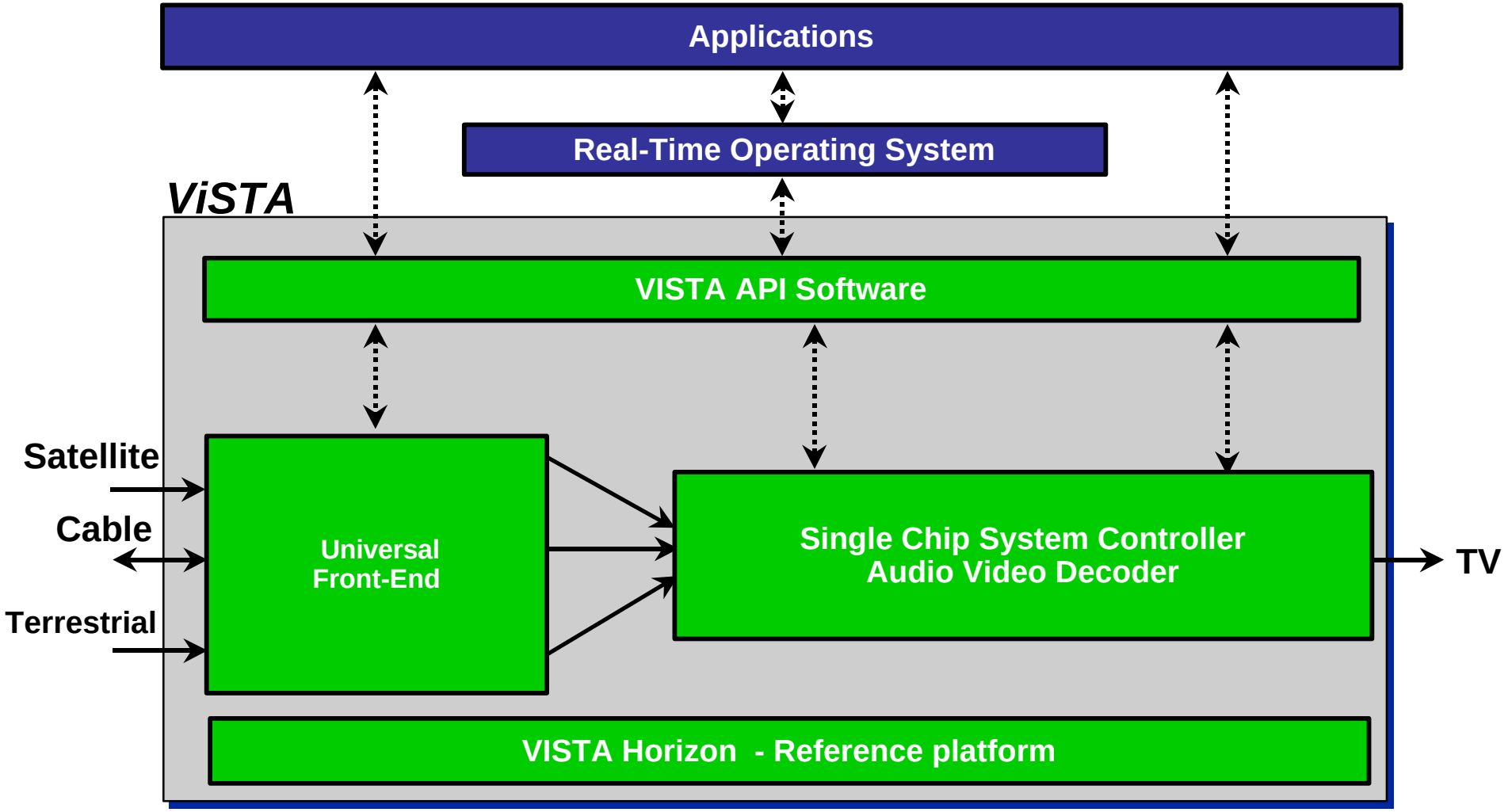
ViSTA 2000 Architecture



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ASIC Business Unit

- **Deliver worldclass service to customers in new and emerging markets.**
- **Dedicated resources reduce schedule risk. These resources bring all of VLSI's IP, physical design and manufacturing capabilities to new VLSI customers.**
- **Reduced design cycle times are supported through the Velocity development platform.**

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VLSI-The ASIC supplier of choice

- **20 years of experience in ASIC design drives fast, proven and flexible design and manufacturing processes.**
- **VLSI's worldwide Technical Centers provide an unmatched level of local technical support and ASIC design services**
- **Industry leading experience in ARM integration lowers schedule risk, while ensuring maximum performance. Over 50% of merchant ARM designs completed by VLSI**
- **VLSI focus on advanced design methodologies reduces development time and risk in developing right first time silicon**
  - **Deconfigurable Rapid Silicon Prototypes for embedded processor designs to enable concept to silicon in 12 weeks**
  - **HDLi compiler for area and performance optimized compiled cells**
  - **HDLi templates for configurable reusable IP**
- **Leading edge process technology, HD cell library and HDLi compiler combine to deliver the industry's top density. High density translates to lower power, higher performance and lower cost**

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Conclusion

System & Applications Expertise

- **Help Customers Define As Well As Efficiently Implement Their Systems on a Chip When Needed**
- **System Architecture and Design**
  - **Wireless**
  - **Digital entertainment**
  - **WAN/LAN**
  - **PC Core Logic and Audio**
- **Hundreds of ASIC Designs**
- **Unique Features**
  - **Security**
  - **ARM DSP and Multiprocessor based designs**
  - **Mixed Signal designs**
  - **High Speed I/O & Clock Recovery**

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Why an Integrated ASIC Supplier?

- **As an Integrated Supplier VLSI Gets You to Revenue Faster, With Less Risk and Lower Overall Cost of Ownership.**
- **Reduce Risk by Providing a Single Point of Contact From Start to Finish.**
- **20 Years Experience in IC Development, Design and Manufacturing**
- **The Right Tools for the Right Job**
  - **HDL Integrator (HDLi) design tool for IP reuse**
  - **Design Integrator for seamless integration of industry leading tools**
  - **Rapid Silicon Prototyping design style uses hardware and software co-development, reduces risk and gets your system level silicon to market faster**
  - **Factory flows and logistics optimized for fast prototype turn and flexible production ramp**
- **Tools, Libraries and IP Optimized for VLSI Processes**
  - **Yields industry's highest density designs while optimizing power, speed and cost**
  - **Reusable IP and design libraries qualified and optimized for VLSI processes**
- **Customers Can Design IC's Without Getting in the Chip Business**

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Summary

- **VLSI Enables the Fastest Time to Volume Through:**
  - **Expert, local design services located worldwide**
  - **Advanced design & logistics processes and tools that drive the shortest time to volume**
  - **A broad offering of reusable IP**
  - **Higher performance, lower power & cost designs through advanced compilers and high density processes**
- **Customers Who Deliver Added Value in Their Products Through Custom Silicon Design Cannot Afford the Risk of Schedule Delay.**
- **Today, VLSI Helps Many Customers, Including Those Below, Hit Their Market Windows in Less Time.**

- Apple	- HP
- Ericsson	- Thomson Multimedia
- Silicon Graphics	- Sega

- **If First-time-right Silicon Is Strategic to Your Success, Then VLSI Is Your ASIC Partner of Choice**

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